IN THE CLAIMS

Please cancel claims 1-14 without prejudice or disclaimer.

Please add claims 23-29.

**Listing of Claims:**

Claims 1-14 (cancelled)

Claim 15 (original) A method for maintaining Translation Lookaside Buffer (TLB) consistency in a system comprising a shared memory and a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein each of said plurality of direct memory access controllers comprises a TLB, the method comprising the steps of:

invalidating a copy of a page table entry that was updated in a particular TLB of a direct memory access controller associated with a particular processing unit by said particular processing unit;

broadcasting a TLB invalided entry instruction to each of said plurality of processing units other than said particular processing unit by said particular processing unit;

determining whether to invalidate any entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit; and

issuing a synchronization instruction to each of said plurality of processing units other than said particular processing unit by said particular processing unit.

Claim 16 (original) The method as recited in claim 15, wherein each of said plurality of processing units other than said particular processing unit that received said TLB invalidated entry instruction is configured to search through the entries of said TLB's of

its associated direct memory access controllers to determine whether there are any invalid entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit.

Claim 17 (original) The method as recited in claim 15, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit is configured to search through the entries of its associated TLB's to determine whether there are any invalid entries in each of said TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit.

Claim 18 (original) The method as recited in claim 16, wherein each of said plurality of processing units other than said particular processing unit invalidates any invalid entries in said TLB's of its associated direct memory access controllers.

Claim 19 (original) The method as recited in claim 17, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit invalidates any invalid entries in its associated TLB's.

Claim 20 (original) The method as recited in claim 15 further comprising the step of:

issuing an acknowledgment to said particular processing unit that any invalid entries were invalidated.

Claim 21 (original) The method as recited in claim 20, wherein each of said plurality of processing units other than said particular processing unit issues an acknowledgment to said particular processing unit that any invalid entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit were invalidated.

Claim 22 (original) The method as recited in claim 20, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit issues an acknowledgment to said particular processing unit that any invalid entries in its associated TLB's were invalidated.

Claim 23 (new) A system, comprising:

a shared memory;

a first and a second processing element coupled to said shared memory, wherein said first processing element comprises:

a first processing unit, wherein said first processing unit comprises a translation lookaside buffer (TLB);

a first direct memory access controller coupled to said first processing unit, wherein said first direct memory access controller comprises a TLB; and

a first plurality of attached processing units coupled to said first direct memory access controller;

wherein said second processing element comprises:

a second processing unit, wherein said second processing unit comprises a TLB;

a second direct memory access controller coupled to said second processing unit, wherein said second direct memory access controller comprises a TLB; and

a second plurality of attached processing units coupled to said second direct memory access controller;

wherein said first processing unit comprises:

logic for invalidating a copy of a page table entry that was updated in a TLB in one of said first processing unit and said first direct memory access controller; and

logic for broadcating a TLB invalidated entry instruction to said second processing unit.

Claim 24 (new) The system as recited in claim 23, wherein said second processing unit comprises:

logic for invalidating any invalid entries in said TLB of one of said second processing unit and said second direct memory access controller.

Claim 25 (new) The system as recited in claim 24, wherein said second processing unit comprises:

logic for issuing an acknowledgment of invalidating any invalid entries in said TLB of one of said second processing unit and said second direct memory access controller to said first processing unit.

Claim 26 (new) The system as recited in claim 25, wherein said first processing unit comprises:

logic for issuing one or more synchronization instruction to said second processing unit.

Respectfully submitted,

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